APPLICATION NOTE

Inductive Load Test Losses

Purpose

The ITC55X00 UIS testers provide significant test time improvements over the previously offered ITC5510 models. This application note describes the areas of major test times improvements.

ITC55100/55300 Test Time Improvements

The ITC55100 and ITC55300 UIS test systems provide significant improvements in test times from the ITC5510 models previously offered. One major improvement is obtained by the ability to charge the inductor at a higher voltage than the breakdown voltage of the DUT without any damage to the DUT and without sacrificing the ability to test the leakage current of the DUT.

The improvement is provided by the addition of a separate programmable leakage test voltage which can be any value up to the value of the drain voltage supply. The internal high voltage, high speed switch disconnects the drain supply voltage from the DUT until the start of the inductor charging cycle when the DUT is turned on. Before the drain voltage is connected, the leakage test circuit can test the DUT for excess leakage at a voltage below the breakdown voltage of the DUT and then with the DUT turned on the inductor can be charged with a voltage that could be several times greater than the DUT breakdown voltage.

A simplified set of waveforms for the ITC55100 is shown in Figure-1. The inductor charging time is labeled T1 and the inductor discharge (avalanche) time is labeled T2. If the effects of resistance in the circuit are ignored, the calculations for T1, T2 and the Energy (E) stored in the inductor are very simple.

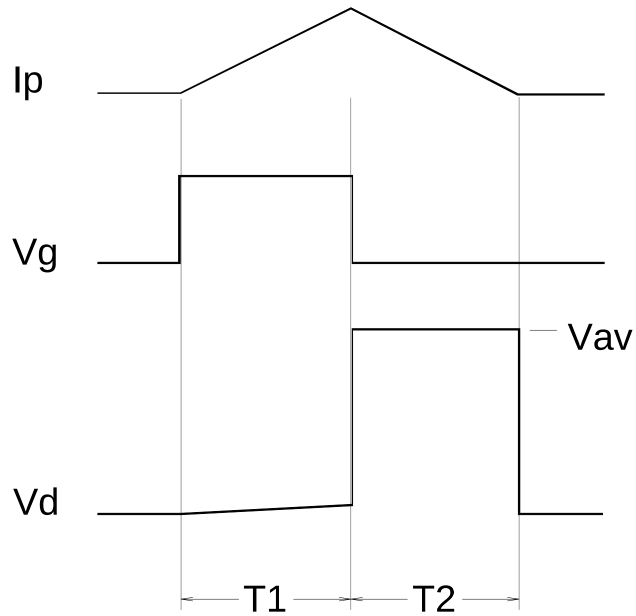

Figure 1: Simplified T1 and T2 Waveforms For the ITC55100

T1 = L*Ip/2*Vdd	Inductor Charge Time
T2 = L*Ip/Vav	Inductor Discharge Time
E = ½*L*I^2	Energy Stored in Inductor

L = Inductance in Henries
Ip = Peak Current in Amperes
Vdd = Drain Supply Voltage in Volts
Vav = Avalanche Voltage in Volts

NOTE: T1 time calculation is not dependent on any device parameter using this equation.*

The T2 time is affected by the avalanche voltage of the DUT (Vav) but is not affected by the drain supply voltage (Vdd). The energy (E) stored in the inductor is also not affected by the drain supply voltage (Vdd). The test conditions actually applied to the device are completely unaffected by the value of Vdd. The same avalanche voltage, avalanche current and avalanche energy is applied regardless of the value of Vdd. This allows the Vdd to be increased for faster T1 times which will reduce overall test time without affecting the actual device test conditions in any way.

The decrease in test times will be most apparent for low voltage, high current devices. Table 1 shows the test times for some typical high current 30 volt devices with the Vdd set at 25 volts and at 150 volts. The “DELTA” column is the reduction in test time possible by setting the Vdd supply to 150V rather than 25V. On the 30V device, the T2 times will only be slightly less than the T1 times, so the savings in total test time are about 40%. This is equivalent to a 67% increase in throughput for the UIS test.

TEST PARAMETERS				T1 TIME (MS)		
PART	**E (mJ)**	**L (uH)**	**Ip (A)**	**Vdd = 25V**	**Vdd = 150V**	**DELTA**
IRF3703	1700	56	59	69.6	11.6	58.0
IRF1503	980	589	76	89.5	14.9	74.6
IRF3707	213	110	62	13.6	2.3	11.4
IRFU3303	95	590	18	17.7	3.5	14.2

Table 1: Test Time Improvement Chart

* In actual fact, the Vds(on) voltage of the power MOSFET under test will affect the charging time slightly by decreasing the voltage across the inductor and lengthen the T1 time accordingly. To be more precise, we could add in a Vds(on) term which would subtract from Vdd, however, it would be a variable since the current is changing during the T1 time. It is possible to use the value of Vds(on) at ½ Ip to get a slightly more accurate number, however, in most cases the Vds(on) is considerably less than the Vd so the effect is minimal.

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